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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/715,593	11/19/2003	David Walter Flynn	550-488	6450

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EXAMINER	
PRETLOW, DEMETRIUS R	
ART UNIT	**PAPER NUMBER**
2863	

DATE MAILED: 01/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/715,593	FLYNN, DAVID WALTER	
	Examiner	Art Unit	
	Demetrius R. Pretlow	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,15-17,21-25,35-37 and 41* is/are rejected.

7)☒ Claim(s) *6-14,18-20,26-34,38-40* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the mapping circuit in claims 1, 21 and the plurality of mapping circuits in claims 5 and 25 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 11 and 31 recites the limitation "said configuration values" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claims 16 and 36 recites the limitation "said current operation signal" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claims 17 and 37 recites the limitation " said current operation signal " in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4,15-17,21-24,35-37 and 41 are rejected under 35 U.S.C. 102(e) as being anticipated by Cooper (US 6,823,516). Given the broadest reasonable interpretation in reference to claims 1 and 21, Cooper (US 6,823,516) teach a processor (12) operable to perform data processing operations under control of program instructions, said processor being operable under program instructions control to

generate a performance level request signal indicative of a desired data processing performance level of said processor. Cooper teach determining the state change required and write to the performance control register state number for new CPU state and performing the state transition event which suggests that a request was made to change the state. Note column 11, lines 11-17. Cooper does not explicitly teach a mapping circuit (which appears to be inherent to the invention of Cooper), the examiner interprets mapping as transforming or converting . Cooper teach the state change required and write to the performance control register state number for new CPU state and performing the state transition event which suggests that a request was made to change the state. Note column 11, lines 11-17. This suggests the request signal mapping circuit (inherent) operable to map said performance level request signal into a control signal supplied to one or more further circuits to control operation of said one or more further circuits so as to support said desired data processing performance level of said processor such that said program instructions controlling generation of said performance level request signal are independent of how said one or more further circuits are controlled to meet said desired data processing performance level.

In reference to claims 2 and 22, Cooper teach in the automatic mode of operation, CPU speed is adjusted based on the demand placed on the CPU. When the system crosses a threshold of non-idleness for a specified time period, the next higher CPU speed is selected automatically. Note column 23, lines 38-44)This suggests wherein said one or more further circuits include a clock generator (inherent to adjusting CPU speed) operable to generate a clock signal (inherent to adjusting CPU speed) with

a selectable clock frequency, said clock signal being supplied to said processor to drive said processing operations such that data processing performance of said processor varies in dependence upon which clock frequency is selected.

In reference to claims 3 and 23, Cooper teach processor 12 shifts between performance states both as a function of a voltage level applied to the power input of processor 12 and as a function of the frequency of a periodic waveform applied to the clock input of processor 12. Note column 3, lines 56-60. and performance control logic 16 (voltage controller) simply modifies the core frequency to bus frequency ratio seen by processor 12, in order to move to a different performance state. Note column 4, lines 11-14. In another embodiment, performance control logic 16 provides a continuous range of voltage levels and adjusts the performance level of processor 12 as a function of a voltage level or a clock frequency supplied by performance control logic 16. This suggests a voltage controller operable to generate a power supply signal, said power supply signal being supplied to said processor at a selectable voltage level, different voltage levels allowing different switching speeds within said processor such that a maximum usable data processing performance varies in dependence upon which voltage level is selected.

In reference to claims 4 and 24, Cooper teach a performance-state-enabled system can use one or more active thresholds to engage active thermal management at the appropriate temperatures. Passive thresholds (indicated by _PSV objects) define a temperature at which the power of one or more CPUs should be reduced in order to

cool a given thermal zone which suggests wherein said control signal is a thermometer coded value. Note column 32, lines 35-40.

In reference to claims 15 and 35, Cooper teach wherein at least while responding to a change in said performance control signal, said further circuit is operable to generate a current operation signal indicative of current operation of said further circuit. Note column 26, lines 37-52.

In reference to claims 16 and 36, Cooper teach current operation signal is indicative of a maximum power supply voltage of that can currently be supported by said voltage controller. Note column 5, lines 32-38.

In reference to claims 17 and 37, Cooper teach currently operation signal is indicative of a clock frequency that is currently being generated by said clock generator. Note column 22, lines 60-62.

In reference to claim 41, Cooper teach a computer program product contating program instructions for controlling a processor to operate in accordance with the method as claimed in claim 22. Note claim 21.

Allowable Subject Matter

In reference to claims 5 and 25 the prior art of record does not teach the inclusion of the limitations of an a plurality of processors and mapping circuits operable to generate respective thermometer coded values which are logically combined to produce a combined thermometer coded value to control at least one of said one or

more circuits. It is these limitations found in each of the claims, as they are **claimed in the combination**, that has not been found, taught or suggested by the prior art of record.

In reference to claims 6,7, 26 and 27 the prior art of record does not teach the inclusion of the limitations of an mapping circuit performs a many to one mapping between performance level request signal values and corresponding control signal values. It is these limitations found in each of the claims, as they are **claimed in the combination**, that has not been found, taught or suggested by the prior art of record.

In reference to claims 8 and 28 the prior art of record does not teach the inclusion of the limitations of an wherein performance level supported as controlled by control signal value increases monotonically with performance level request signal value. It is these limitations found in each of the claims, as they are **claimed in the combination**, that has not been found, taught or suggested by the prior art of record.

In reference to claims 9 and 29 the prior art of record does not teach the inclusion of the limitations of an one of said one or more further circuits operates in a different clock domain to said processor. It is these limitations found in each of the claims, as they are **claimed in the combination**, that has not been found, taught or suggested by the prior art of record.

In reference to claims 10 and 30 the prior art of record does not teach the inclusion of the limitations of an at least one of said one or more further circuits is configured with one or more configuration values specifying how said further circuit should respond to different control signal values. It is these limitations found in each of

the claims, as they are **claimed in the combination**, that has not been found, taught or suggested by the prior art of record.

In reference to claims 11 and 31 the prior art of record does not teach the inclusion of the limitations of an configuration vales specify voltage levels corresponding to different control signal values. It is these limitations found in each of the claims, as they are claimed in the combination, that has not been found, taught or suggested by the prior art of record.

In reference to claims 12,14,32 and 34 the prior art of record does not teach the inclusion of the limitations of an wherein while responding to a change in performance control signal corresponding to a change from a first desired data processing performance level to a second desired data processing performance level, said one or more further circuits are operable to support data processing at least one intermediate data processing performance level and said processor temporarily operates at said at least one intermediate data processing performance level during said change. It is these limitations found in each of the claims, as they are **claimed in the combination**, that has not been found, taught or suggested by the prior art of record.

In reference to claims 13 and 33 the prior art of record does not teach the inclusion of the limitations of an wherein, in response to an increase in desired data processing performance level, said clock generator increases clock signal frequency to an intermediate clock signal frequency when said voltage controller is generating a power signal with a voltage level sufficient to support said intermediate clock signal

frequency.. It is these limitations found in each of the claims, as they are **claimed in the combination**, that has not been found, taught or suggested by the prior art of record.

In reference to claims 18,19,38,39 the prior art of record does not teach the inclusion of the limitations of an where said clock generator is operable to generate a clock signal with one or mom permanently available clock signal frequencies and one or more selectively available clock signal frequencies. It is these limitations found in each of the claims, as they are **claimed in the combination**, that has not been found, taught or suggested by the prior art of record.

In reference to claims 20 and 40 the prior art of record does not teach the inclusion of the limitations of an in response to an increase in desired data processing performance level, said clock generator increases clock signal frequency when said voltage controller generates a current operation signal indicative of a generation of said power signal with a voltage level sufficient to support an increased clock signal frequency. It is these limitations found in each of the claims, as they are **claimed in the combination**, that has not been found, taught or suggested by the prior art of record.

Response to Arguments

Applicant's arguments with respect to claims 1-41 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Demetrius R. Pretlow whose telephone number is (571) 272-2278. The examiner can normally be reached on Mon.-Fri. 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571) 272-2269. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Demetrius R. Pretlow 1/3/05

Patent Examiner

MICHAEL NGHIEM
PRIMARY EXAMINER